

In the Claims:

Please amend claim 31. The claims are as follows:

1-30. (Cancelled)

31. (Currently amended) A semiconductor device, comprising:

a substrate;

a first wiring level on a top surface of the substrate, said first wiring level comprising alternating layers of a first dielectric material and a second dielectric material, said layers of the first dielectric material comprising a plurality of layers of the first dielectric material, said layers of the second dielectric material comprising a plurality of layers of the second dielectric material;

a first trench and a second trench each extending through the first wiring level, from a top surface of the first wiring level to the top surface of the substrate;

a first layered structure comprising a portion of all of the alternating layers, said first layered structure being disposed between the first and second trenches and extending from the top surface of the first wiring level to the top surface of the substrate; and

a dielectric liner conformally deposited on a bottom wall of the first trench, a sidewall of the first trench, a sidewall of the second trench, and a bottom wall of the second trench,

wherein the first dielectric material within the first layered structure in each layer of first dielectric material is disposed between a first air gap and a second air gap within the first layered structure in each layer of first dielectric material,

wherein the first and second air gaps within the first layered structure in each layer of first

dielectric material are respectively bounded by the liner on the sidewall of the first and second trenches,

wherein the second dielectric material within the first layered structure in each layer of second dielectric material is in direct mechanical contact with the sidewall of the first trench and the sidewall of the second trench.

32. (Previously presented) A semiconductor device, comprising:

a substrate;

a first wiring level on a top surface of the substrate, said first wiring level comprising alternating layers of a first dielectric material and a second dielectric material, said layers of the first dielectric material comprising a plurality of layers of the first dielectric material, said layers of the second dielectric material comprising a plurality of layers of the second dielectric material;

a first trench and a second trench each extending through the first wiring level, from a top surface of the first wiring level to the top surface of the substrate;

a first layered structure comprising a portion of all of the alternating layers, said first layered structure being disposed between the first and second trenches and extending from the top surface of the first wiring level to the top surface of the substrate; and

a continuous dielectric liner conformally deposited on a bottom wall of the first trench, a sidewall of the first trench, a top surface of the first layered structure, a sidewall of the second trench, and a bottom wall of the second trench,

wherein the first dielectric material within the first layered structure in each layer of first dielectric material is disposed between a first air gap and a second air gap within the first layered

structure in each layer of first dielectric material,

wherein the first and second air gaps within the first layered structure in each layer of first dielectric material are respectively bounded by the liner on the sidewall of the first and second trenches,

wherein the second dielectric material within the first layered structure in each layer of second dielectric material is in direct mechanical contact with the sidewall of the first trench and the sidewall of the second trench.

33. (Previously presented) The semiconductor device of claim 32, further comprising a first conductive material filling the first and second trenches and extending above and outside the first and second trenches.

34. (Previously presented) A semiconductor device, comprising:

a substrate;

a first wiring level on a top surface of the substrate, said first wiring level comprising alternating layers of a first dielectric material and a second dielectric material, said layers of the first dielectric material comprising a plurality of layers of the first dielectric material, said layers of the second dielectric material comprising a plurality of layers of the second dielectric material;

a first trench and a second trench each extending through the first wiring level, from a top surface of the first wiring level to the top surface of the substrate;

a first layered structure comprising a portion of all of the alternating layers of the first wiring level, said first layered structure disposed between the first and second trenches and

extending from the top surface of the first wiring level to the top surface of the substrate;

a first dielectric liner conformally deposited on a bottom wall and a sidewall of the first trench and a second dielectric liner conformally deposited on a bottom wall and a sidewall of the second trench;

a first conductive material filling the first and second trenches to form a first wire in the first trench and a second wire in the second trench, wherein a top surface of the first wire, a top surface of the first layered structure, and a top surface of the second wire are coplanar,

wherein the first dielectric material within the first layered structure in each layer of first dielectric material is disposed between a first air gap and a second air gap within the first layered structure in each layer of first dielectric material,

wherein the first and second air gaps within the first layered structure in each layer of first dielectric material are respectively bounded by the liner on the sidewall of the first and second trenches,

wherein the second dielectric material within the first layered structure in each layer of second dielectric material is in direct mechanical contact with the sidewall of the first trench and the sidewall of the second trench.

35. (Previously presented) The semiconductor device of claim 34, further comprising an insulative layer on the first wiring level, wherein the insulative layer is in direct mechanical contact with the top surface of the first wire, the top surface of the first layered structure, and the top surface of the second wire.

36. (Previously presented) The semiconductor device of claim 35, further comprising a second wiring level on a top surface of the insulative layer and in direct mechanical contact with the top surface of the insulative layer, said second wiring level comprising alternating layers of a third dielectric material and a fourth dielectric material, said layers of the third dielectric material comprising a plurality of layers of the third dielectric material, said layers of the fourth dielectric material comprising a plurality of layers of the fourth dielectric material, wherein a top surface of the second wiring level is further from the top surface of the insulative layer than is any other surface of the second wiring level.

37. (Previously presented) The semiconductor device of claim 36, further comprising a third trench extending through the second wiring level and the insulative layer, from the top surface of the second wiring level to the top surface of the first wire.

38. (Previously presented) The semiconductor device of claim 36, further comprising:

- a third trench extending through the second wiring level and the insulative layer, from the top surface of the second wiring level to the top surface of the first wire, wherein the third trench is a dual damascene structure being wider in the second wiring level than in the insulative layer;
- a fourth trench extending through the second wiring level, from the top surface of the second wiring level to the top surface of the insulative layer; and
- a second layered structure comprising a portion of all of the alternating layers of the second wiring level, said second layered structure disposed between the third and fourth trenches and extending from the top surface of the second wiring level to the top surface of the insulative

layer.

39. (Previously presented) The semiconductor device of claim 38, further comprising:

a continuous dielectric liner conformally deposited on a bottom wall of the third trench, a sidewall of the third trench, a top surface of the second layered structure, a sidewall of the fourth trench, and a bottom wall of the fourth trench,

wherein the third dielectric material within the second layered structure in each layer of third dielectric material is disposed between a third air gap and a fourth air gap within the second layered structure in each layer of third dielectric material,

wherein the third and fourth air gaps within the second layered structure in each layer of third dielectric material are respectively bounded by the liner on the sidewall of the third and fourth trenches,

wherein the fourth dielectric material within the second layered structure in each layer of fourth dielectric material is in direct mechanical contact with the liner on the sidewall of the third trench and the liner on the sidewall of the fourth trench.

40. (Previously presented) The semiconductor device of claim 39, further comprising a second conductive material filling the third and fourth trenches and extending above and outside the third and fourth trenches.

41. (Previously presented) The semiconductor device of claim 38, further comprising:

a second conductive material filling the third and fourth trenches to form a third wire in

the third trench and a fourth wire in the fourth trench, wherein a top surface of the third wire, a top surface of the second layered structure, and a top surface of the fourth wire are coplanar,

wherein the third dielectric material within the second layered structure in each layer of third dielectric material is disposed between a third air gap and a fourth air gap within the second layered structure in each layer of third dielectric material,

wherein the third and fourth air gaps within the second layered structure in each layer of third dielectric material are respectively bounded by the liner on the sidewall of the third and fourth trenches,

wherein the fourth dielectric material within the second layered structure in each layer of fourth dielectric material is in direct mechanical contact with the liner on the sidewall of the third trench and the liner on the sidewall of the fourth trench.

42. (Previously presented) The semiconductor device of claim 31,

wherein the first and second air gaps within the first layered structure in each layer of first dielectric material directly interface with an interior space of the first and second trenches respectively, and

wherein the second dielectric material within the first layered structure in each layer of second dielectric material is in direct mechanical contact with the interior space of the first and second trenches.

43. (Previously presented) The semiconductor device of claim 32, wherein the first dielectric material within a bottom layer of the alternating layers is in direct mechanical contact with the

substrate.

44. (Previously presented) The semiconductor device of claim 43, wherein a top surface of a top layer of the alternating layers is coplanar with the top surface of the first wiring level, and wherein the top layer comprises the second dielectric material.

45. (Previously presented) The semiconductor device of claim 32, wherein the substrate is a pre-metal dielectric (PMD) substrate, wherein the first dielectric material comprises an organic dielectric material selected from the group consisting of polyarylene ether (SILKTM), parylene (N), parylene (I), Teflon, porous polyarylene ether (SILKTM), porous parylene (N), porous parylene (I) and porous Teflon, and wherein the second dielectric material comprises an inorganic dielectric material selected from the group consisting of OSG, SiO₂, FSG, MSQ, porous OSG, porous SiO₂, porous FSG, and porous MSQ.

46. (Previously presented) The semiconductor device of claim 32, wherein the continuous dielectric liner comprises a material selected from the group consisting of SiCOH, SiO₂, SiN, SiC, and SiCN.

47. (Previously presented) The semiconductor device of claim 34, wherein the first dielectric material within a bottom layer of the alternating layers is in direct mechanical contact with the substrate.

48. (Previously presented) The semiconductor device of claim 47, wherein a top surface of a top layer of the alternating layers is coplanar with the top surface of the first wiring level, and wherein the top layer comprises the second dielectric material.

49. (Previously presented) The semiconductor device of claim 34, wherein the substrate is a pre-metal dielectric (PMD) substrate, wherein the first dielectric material comprises an organic dielectric material selected from the group consisting of polyarylene ether (SILKTM), parylene (N), parylene (F), Teflon, porous polyarylene ether (SILKTM), porous parylene (N), porous parylene (F) and porous Teflon, and wherein the second dielectric material comprises an inorganic dielectric material selected from the group consisting of OSG, SiO₂, FSG, MSQ, porous OSG, porous SiO₂, porous FSG, and porous MSQ.

50. (Previously presented) The semiconductor device of claim 34, wherein the first and second dielectric liners comprise a material selected from the group consisting of SiCOH, SiO₂, SiN, SiC, and SiCN.